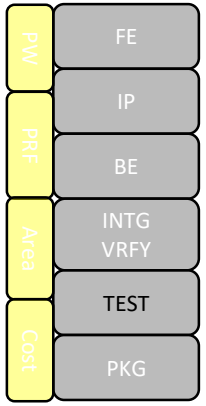
KeyASIC

Test Development, Test Strategy and Good Practice

March 2019

Moscow

Key ASIC Test Services



- In-house HW & SW development
  - Wafer level (CP) & package level (FT)
- Wide experiences in ASIC test
  - RF, mixed signal, analog and digital
- Production management and optimization
  - Yield, quality and cost
- Various tester choices for different performance/cost requirements

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Test Partners

PW
PRF
Area
Cost

FE
IP
BE
INTG
VRFY
TEST
PKG

Chroma

OSE
A partner you can count on
Orient Semiconductor Electronics

Vate 立衛科技股份有限公司
Vate Technology Co.,Ltd.

Testar
LED/SEMICONDUCTOR TEST SERVICES

KYEC

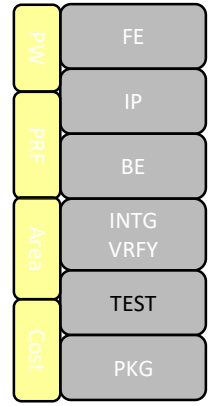
Global Testing Corporation
實邦科技股份有限公司

True
True Test Technology Inc.

TERADYNE

ADVANTEST®

ASIC Test Objectives



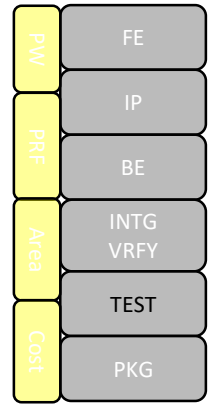
Reliable

Maximize Test Coverage

Cost

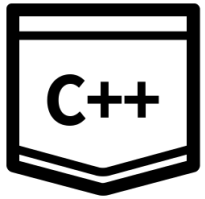
Minimize Test Time

ASIC Test Strategy

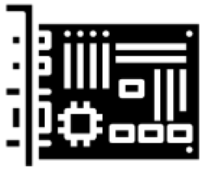


Test Requirement

Tester Selection



Test Program Development



Hardware Development

Silicon Debug

Optimization

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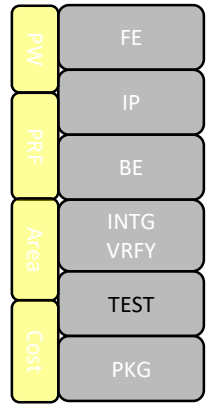
ASIC Test Strategy



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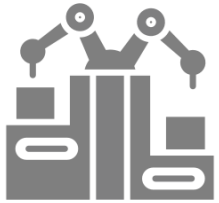
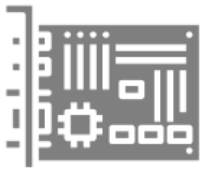


Tester Selection

Test Program Development



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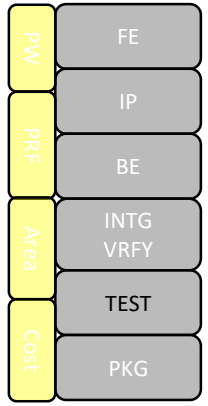
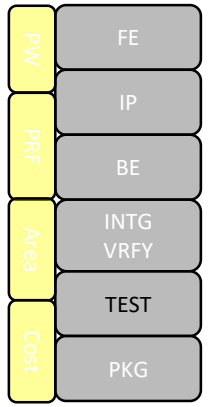
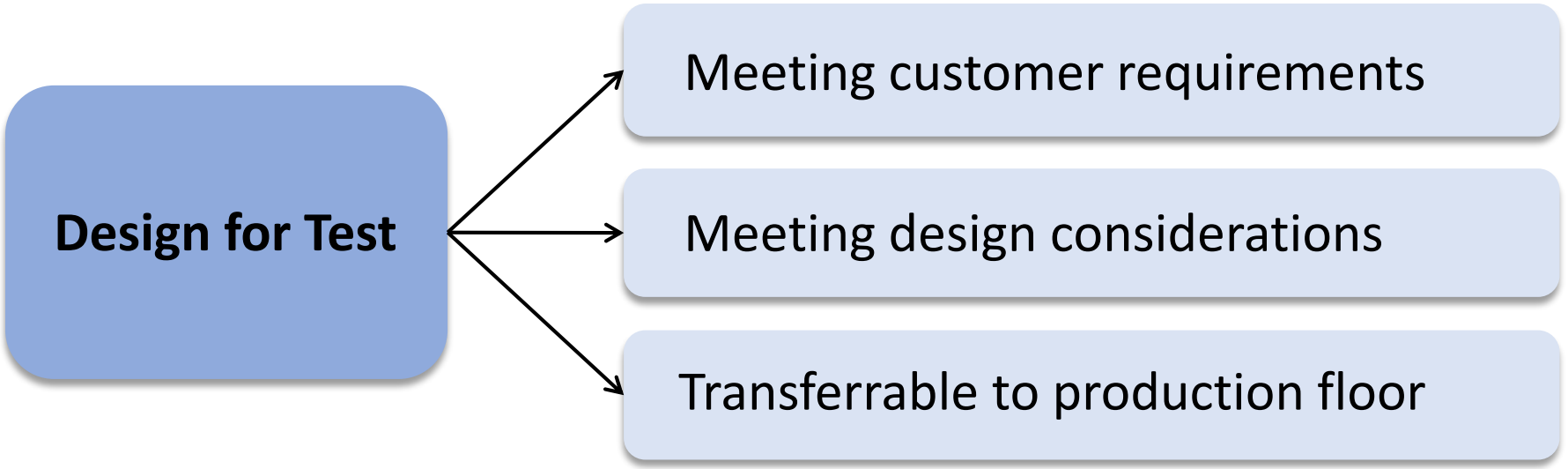


- Cross-functional involvement
  - Customer, design engineer, DFT engineer, test engineer
- Define the level of test coverage required
  - DFT implementation, functional tests
  - Example:
    - To implement I_{DDQ} test, design could incorporate a global signal line that shuts down the current drawing circuitry.
- Number of IO pins, test frequency, temperature
- Finalize test plan

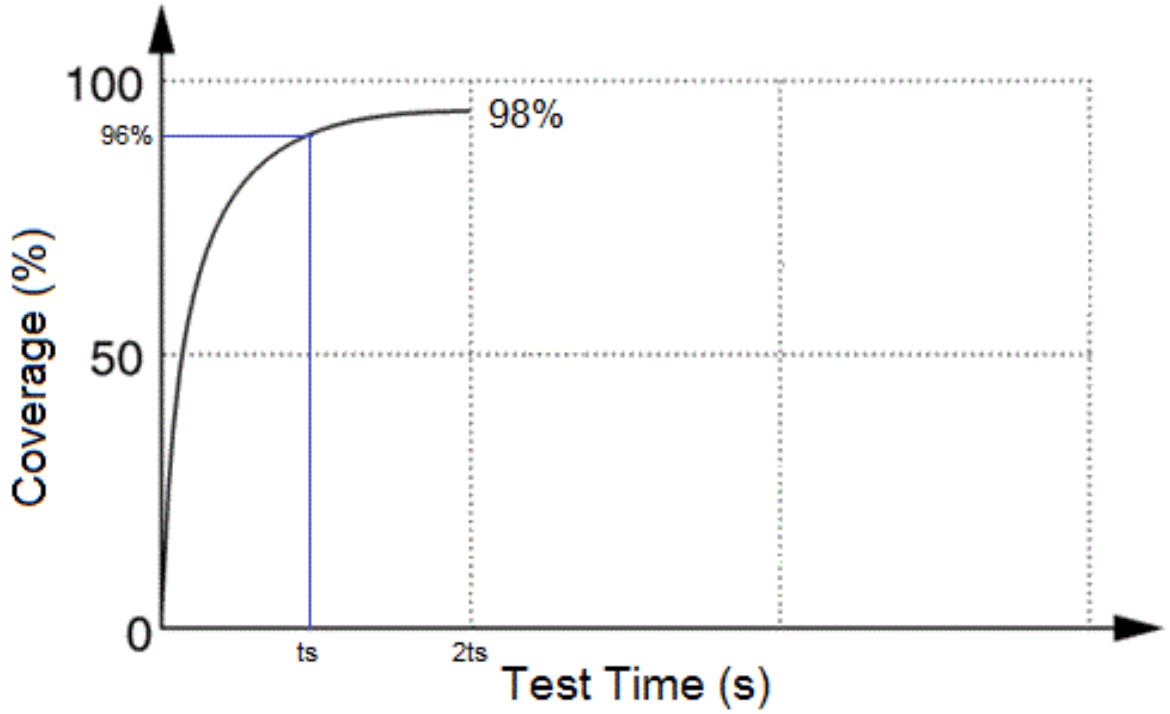
Design for Test



- ATPG scan, Boundary-scan cells and Memory BIST



Stuck –at Coverage vs Test Time



Trade-off between coverage and test time

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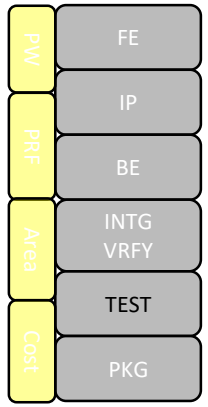
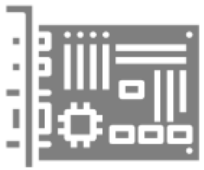
ASIC Test Strategy



Test Requirement

Tester Selection

Test Program Development



Hardware Development

Silicon Debug

Optimization

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Tester Selection

IC Function
Eg: (AD/DA)

Package
Type

Pin Count

Test
Frequency

Vector
Memory

Cost

Availability

PW
PRF
Area
Cost

FE
IP
BE
INTG
VRFY
TEST
PKG

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Tester Selection

PW: FE, IP
PRF: BE
Area: INTG VRFY, TEST
Cost: PKG

Lower Cost → **High Cost**

VLSI Test System
Model 3360-P

- 50 Mhz clock rate, 256 I/O channels
- Up to 32 sites Parallel testing
- Support ADDA, Mixed-signal , LCD ...etc option card
- Flexible Architectures: Slot interchangeable I/O, ADDA, UVI, HVREF ...etc option

VLSI Test System
Model 3380-P

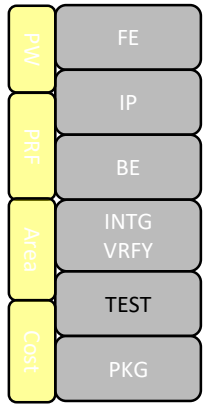
- 100Mhz clock rate, 512 I/O channels (Max to 576 pins)
- Up to 512 sites Parallel testing
- Various VI source
- Flexible Architectures: Slot interchangeable I/O, ADDA, VI source

Advanced SoC/Analog Test System
Model 3680

- Application coverage:MCU, Digital Audio, DTV, STB, DSP, Network Processor and Field, FPGA
- 24 interchangeable slots for digital,analog and mixed-signal applications
- 150 Mbps up to 1Gbps data rate (muxed)

Lower Range → **Advanced**

Tester Selection - Other Factor



- In reality, the testing cost of the tester varies from one test vendor to another
  - Production Capacity
  - Utilization
- The cost by vendor A can be 20-30% cheaper than vendor B
- The benefit of having multiple test vendors in order to maintain cost competitive

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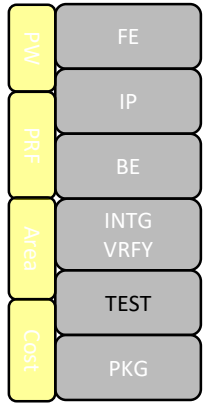
Tester Model



Tester	Clock Rate	Tester	Clock Rate
Credence ASL1000	14 MHz	Teradyne J750EX	200 ~ 400MHz
Chroma 3360P2	50 MHz	Teradyne J750EX-HD	400 ~ 800 MHz
Credence SC312	50 MHz	Teradyne CATALYST	400 MHz
Chroma 3380	100 MHz	Chroma 3680	500 MHz
Chroma 3650	100 MHz	Teradyne Tiger	< 1 GHz
Teradyne J750	200 MHz	Xcerra Diamondx	< 1 GHz
Chroma 3650EX	200 MHz	Advantest V93000	< 1 GHz
KYEC E320	200 MHz	Teradyne UltraFLEX	< 2 GHz
Teradyne Flex	200 MHz		

Tester model which available at our test vendor’s site

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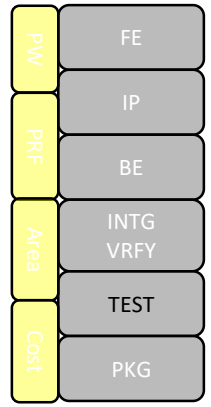
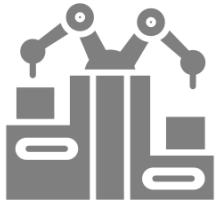
ASIC Test Strategy



Test Requirement



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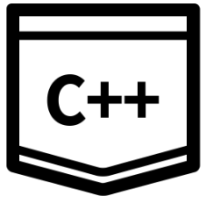
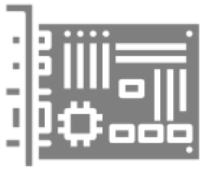


Test Program Development



Hardware Development

Silicon Debug

Optimization

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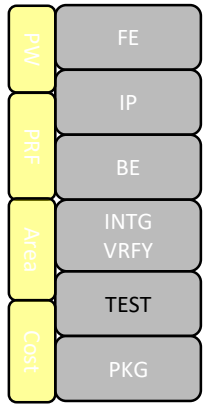
Test Program Development

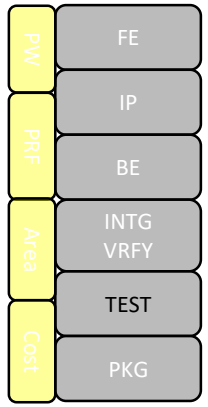


- **Patterns simulation (DFT Engineer/Customer)**
  - **DFT pattern, functional pattern**

- **In-house CP/FT program development**
  - **Test coding, pattern conversion & simulation**
    - **ATPG Scan :** TSTL2/STIL -> .pat
    - **MEMBIST:** EVCD -> .pat
    - **Boundary scan:** EVCD -> .pat

- **Pre-production program validation**

Test Types



Production Test Suite

- Ensure performance meeting design spec
- Long test time
- Eg: Functionality of IP block
- Is it necessary?

Functional Test

Manufacturing Test

- Detect ASIC manufacturing defect
- Short test time
- Eg: Open short, leakage current, scan test, MEMBIST test, boundary scan

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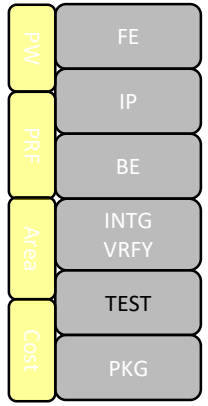
Test Program Flow

- Open Short
- Parametric
- ATPG Scan
- MEMBIST
- Boundary Scan
- Functional Test



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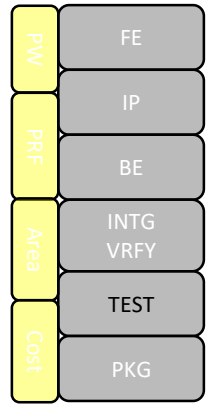
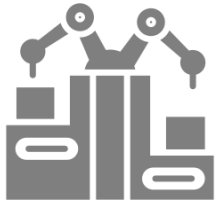
ASIC Test Strategy

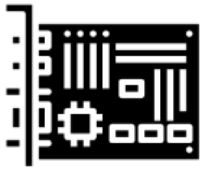


Test Requirement



Tester Selection

Test Program Development



Hardware Development

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Optimization

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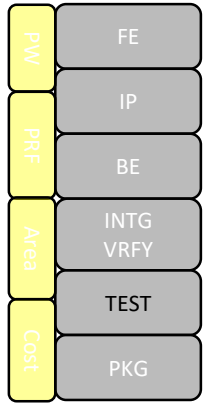
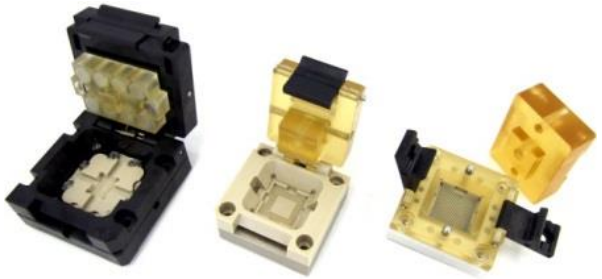
Test Hardware



- Test board design & requirement
  - Power assignment, temperature, speed, relay requirement
  - Challenges -> trace length, noise, cross-talk

- Socket
  - Package type, temperature, life cycle



- Hardware fabrication lead time
  - 2 – 4 months
- Offline hardware check

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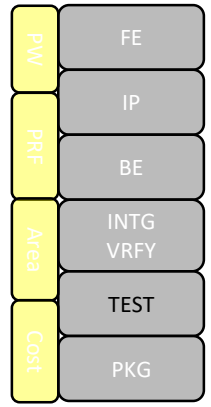
ASIC Test Strategy



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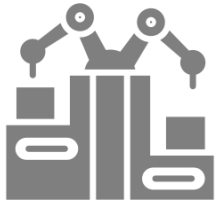

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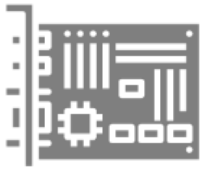

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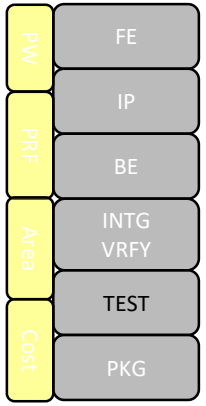

- To ensure the design is working as expected
- Cross functional effort between design engineer, DFT engineer and test engineer
- Steps to a complete silicon debug
  - Start with open short and parametric tests to make sure there is no electrical defect
  - Follow by ATPG Scan test which has the largest fault coverage
  - Bring up the remaining DFT test – MEMBIST and Boundary scan
  - Complete with functional tests

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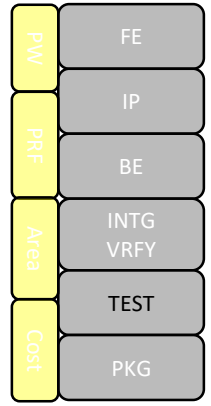
ASIC Test Strategy



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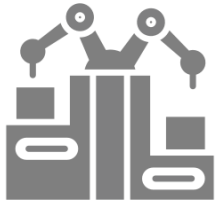

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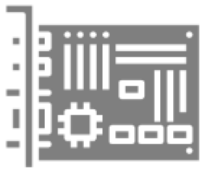

Hardware Development

Silicon Debug

Optimization

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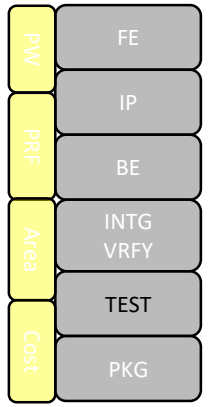
Test Time Optimization



- Improve test program coding
- Reduce wait/delay time
- Reduce relay switching
- Do not power off after pattern completed
- Parallel/group voltage/current measurement
- Increase test frequency
- Pattern removal (low coverage / low DPM)

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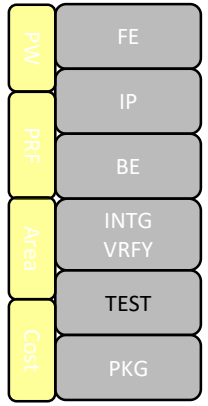
Summary



- A good and effective ASIC testing require early involvement of test engineer
- Cross functional effort is important
  - Customer, design engineer, DFT engineer, test engineer
  - From identifying test requirement to silicon debug
- Each and every strategy in the flow need to be executed correctly
- Production optimization
  - Continuous test cost important

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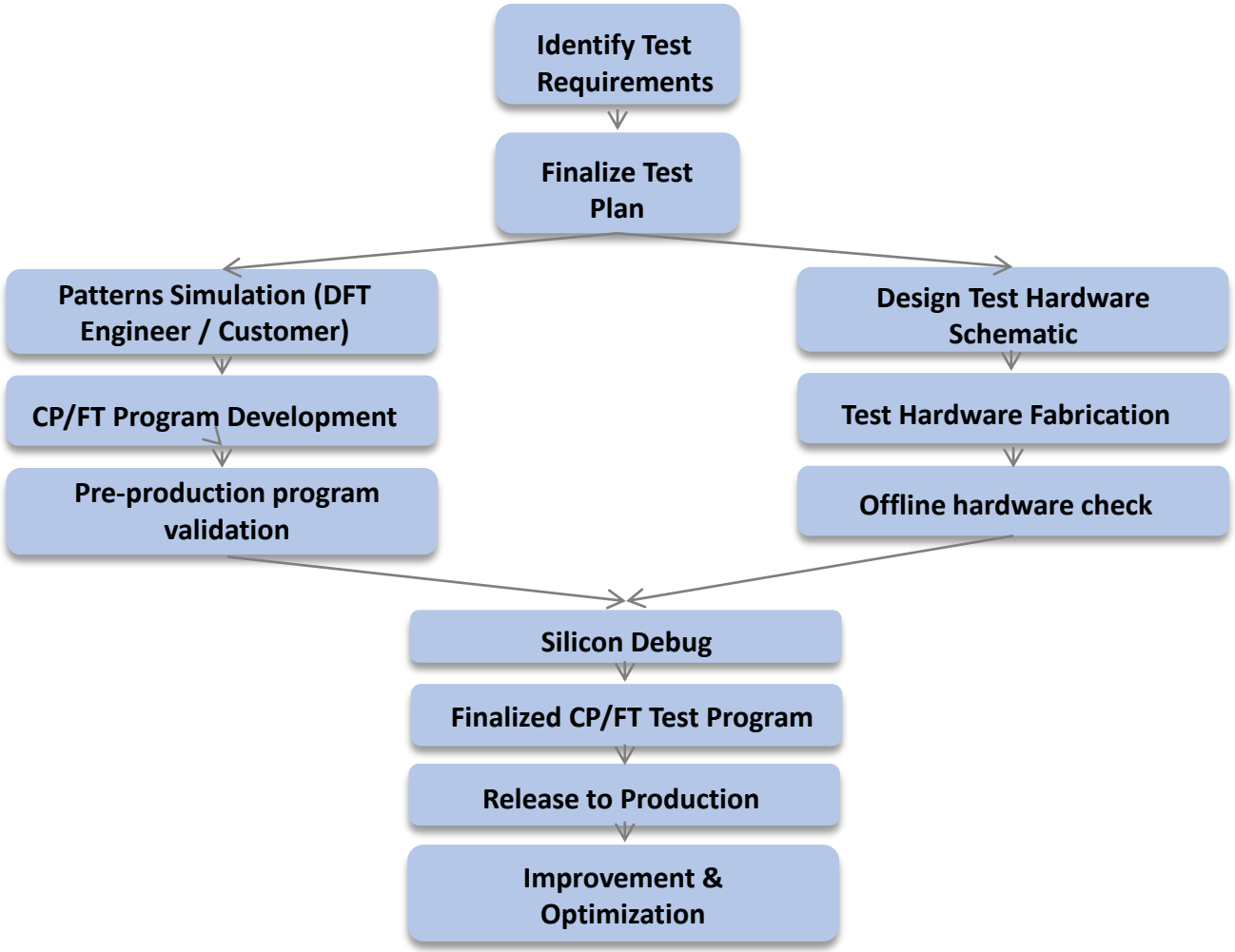
Effective ASIC Testing Flow



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Thank You